

Appl. No. 10/780,188
Response/Amendment dated October 5, 2005
Reply to Office Action of July 8, 2005

Amendments to the Specification:

- a) Please amend the paragraph beginning at the end of page 13 and ending at the top of page 14 to read as follows:

Thus the feedback processor is operable to convert an input signal corresponding to the amplified signal to a feedback signal within the IF band. The feedback processor can include a chopping mixer clocked at a rate to convert an input frequency within the RF band to an output frequency within the IF band. The feedback compensator, if used or needed, is for adjusting a gain, a phase, or a time delay of the feedback signal. This compensation can be adjusted as needed to insure that the control loop remains stable under relevant conditions. The compensation circuit 316 further insures stability by providing for as much as a one clock cycle delay from the input to the encoder 313 through the amplifier 203 and the mixer 325. Additionally the clock signal at 227 can be adjusted (gain, phase, time delay) for the ADC 321, encoder 313, and mixer 323 by the gain/phase adjustment functions 321, 319, 323, respectively. Note that the phase adjustment functions may or may not be required or ~~possible~~ possibly only some of them will be needed. This will depend on the specifics of delays through various portions of the delta sigma modulator or overall amplifier.

- b) Please amend the paragraph beginning at the end of page 16 and ending at the top of page 17 as follows:

Referring to FIG. 5, an illustration or signal/timing diagram that shows the relationship between various signals in the diagram of FIG. 4 will be discussed and described. FIG. 5 shows a clock signal 501, an exemplary ADC output or discrete output signal (D) 503, a Manchester encoder output signal 505 given the clock signal and ADC output signal 503, and an amplified signal 507, such as the signal at ~~205~~ 205, each as a function of clock cycle 509 that varies from cycle 1 to cycle 10. FIG. 5 illustrates the Manchester encoding process in greater detail. On each cycle of the DSM clock 501, the comparator makes a "1" or "0" decision, see 503. The Manchester Encoder encodes the comparator decisions into a continuous-time waveform or encoder output 505 with either the first half of the cycle as "high" (if D is "1") or the second half

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of the cycle as "high" (if D is "0"). This encoding process has the effect of frequency translating signals at the IF frequency to the RF frequency. The PA output or amplified signal 507 is an amplified and phase delayed version of the Manchester Encoder output waveform.

c) Please amend the paragraph beginning at the bottom of page 18 and ending on page 19 to read as follows:

Furthermore the enhanced stability control of the compensation circuit 316, 415 with the A_0 coefficient or feedback path around the ADC 309, 409 provides for an almost full clock cycle delay in the switching PA. As will be appreciated this further reduces the practicalities associated with the implementation of the amplifier or PA. This additional feedback path or compensation circuit allows for a large delay in the PA circuitry without compromising loop stability. This is important because at the RF frequencies of 2GHz, it is tremendously difficult and expensive to reduce the delay or latency of the PA. Without the additional feedback path, the PA delay may make it difficult or impractical to include the PA inside the DSM control loop. If the PA is not inside the control or feedback loop, the feedback signal will have to originate at the input of the PA. In that case, the DSM control loop will not be able to suppress imperfections or non-linearity's of the PA. With the additional feedback path, PA delays of up to a full DSM clock period can be included inside the DSM loop and the tremendous noise suppression capability of the DSM ~~is~~ can be applied to also suppress PA imperfections.